

IN THE CLAIMS:

Please amend claims 10-12 as follows:

1-9. (Canceled)

10. (Currently Amended) An active matrix type display comprising:

a plurality of gate wirings formed on a substrate;

a plurality of data wirings formed on the substrate substantially orthogonal to the gate wirings;

a plurality of pixel electrodes formed in a plurality of pixel areas decided by the gate wirings and the data wirings and arranged in a matrix shape;

a thin film transistor formed in each of the pixel areas and structured planar type having an operating semiconductor layer formed on the substrate, a gate insulating film formed on the operating semiconductor layer, a gate electrode formed on the gate insulating film and connected to one of the gate wirings, first and second semiconductor layers having impurity formed on both sides of the operating semiconductor layer, a source electrode including the first semiconductor layer electrically connected to the pixel electrode via a contact window opened to first and second insulating layers laminated on the first semiconductor layer and the gate electrode; and

a plurality of storage capacitor electrodes using the first semiconductor layer as a first storage capacitor electrode, having a second storage capacitor electrode made of the

17 same ~~material~~ layer as the data wirings and sandwiched between the first insulating film and
18 the second insulating film and connected to a storage capacitor wiring maintained at a
19 predetermined potential, wherein at least a first storage capacitor is structured by the first
20 storage capacitor electrode, the first insulating film and the second storage capacitor
21 electrode, and a second storage capacitor is structured by the second storage capacitor
22 electrode, the second insulating film and the pixel electrode.

1 11. (Currently Amended) An active matrix type display comprising:
2 a plurality of gate wirings formed on a substrate;
3 a plurality of data wirings formed on the substrate substantially orthogonal to
4 the gate wirings;
5 a plurality of pixel electrodes formed in a plurality of pixel areas decided by the
6 gate wirings and the data wirings and arranged in a matrix shape;
7 a thin film transistor formed in each of the pixel areas and structured planar
8 type having an operating semiconductor layer formed on the substrate, a gate insulating film
9 formed on the operating semiconductor layer, a gate electrode formed on the gate insulating
10 film and connected to one of the gate wirings, first and second semiconductor layers having
11 impurity formed on both sides of the operating semiconductor layer, a source electrode
12 including the first semiconductor layer electrically connected to the pixel electrode via a
13

13 contact window opened to first and second insulating layers laminated on the first
14 semiconductor and the gate electrode;

15 an impurity semiconductor layer formed isolated from the first semiconductor
16 layer on the substrate and made of the same material as the first semiconductor layer; and

17 a plurality of storage capacitor electrodes using the ~~first~~ impurity
18 semiconductor layer as a first storage capacitor electrode, having a second storage capacitor
19 electrode made of the same ~~material~~ layer as the data wirings and sandwiched between the
20 first insulating film and the second insulating film and connected to a storage capacitor
21 wiring maintained at a predetermined potential, wherein at least a first storage capacitor is
22 structured by the first storage capacitor electrode, the first insulating film and the second
23 storage capacitor electrode, and a second storage capacitor is structured by the second storage
24 capacitor electrode, the second insulating film and the pixel electrode.

1 12. (Currently Amended) An active matrix type display comprising:
2 a plurality of gate wirings formed on a substrate;
3 a plurality of data wirings formed on the substrate substantially orthogonal to
4 the gate wirings;
5 a first, a second and a third insulating film formed on the gate wirings;
6 a pixel electrode formed in a pixel decided by the gate wirings and the data
7 wirings;
8

8 a thin film transistor formed in the pixel and having a gate electrode connected
9 to one of the gate wirings, a source electrode connected to the pixel electrode, and a drain
10 electrode connected to the data wirings;

11 a first storage capacitor electrode formed between the first insulating film and
12 the second insulating film in an area of the gate wiring for previous pixel to the pixel and
13 connected to the pixel electrode; and

14 second storage capacitor electrode also serving as a storage capacitor wiring
15 formed between the second insulating film and the third insulating film in the area of the gate
16 wiring, and having a peripheral area overlapping a an entire perimeter area of the pixel
17 electrode when observing from a direction perpendicular to the substrate;

18 wherein a first storage capacitor is structured by the first storage capacitor
19 electrode, the second insulating film and the second storage capacitor electrode, and a second
20 storage capacitor is structured by the second storage capacitor electrode, the third insulating
21 film and the pixel electrode.

1 13. (Previously Presented) An active matrix type display as set forth in
2 claim 12, wherein a third storage capacitor is structured by the first storage capacitor
3 electrode, the first insulating film and the gate wiring.

14. (Canceled)

15. (Previously Presented) An active matrix type display as set forth in claim 12, wherein the second storage capacitor electrode also serves as a shading film.